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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/664,981	09/22/2003	Chun-Chi Lee	LEEC3073/EM	4969

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EXAMINER	
CHU, CHRIS C	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 04/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/664,981	LEE ET AL.
	Examiner	Art Unit
	Chris C. Chu	2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 January 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1, 3 - 5, 17, 28 - 44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 3 - 5, 17, 28 - 44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 September 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's amendment filed on January 24, 2005 has been received and entered in the case.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the limitation of the first and second conductive devices are conductive wires, and the back surface of the first and second semiconductor chips face and connect to the upper and lower surfaces of the substrate via the thermal enhance layer in claims 42 and 44 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the

renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claims 28, 36, 40 and 44 are objected to because of the following informalities:

a. In claim 28, line 17, "surfaces" should be --surface--.

b. In claim 36, line 3, "co" should be --of--.

c. In claim 40, line 2, "the bonding" should be --the second bonding--.

d. In claim 44, incomplete sentence. For the examining purpose, Examiner completes the sentence by adding --thermal enhance layer.-- after "via the" in line 3.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 33 and 35 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a. In claim 33, line 2, "the semiconductor chip" lacks antecedent basis, because there are two semiconductor chips.

b. In claim 35, lines 11 and 12, "the bonding pads" lacks antecedent basis, because there are two sets or groups of bonding pads.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1 and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Shin et al. (U. S. Pat. No. 6,395,578).

Regarding claim 1, Shin et al. discloses in e.g., Fig. 7D and column 9, lines 33 – 37 a semiconductor package, comprising:

- a substrate (10 in Fig. 7A; column 9, line 9) having an upper surface and a lower surface opposed to the upper surface;
- a semiconductor chip (30; column 9, line 15) having an active surface (at the surface that has pads), a back surface opposed to the active surface and a plurality of bonding pads (31; column 9, line 17) formed on the active surface;
- a plurality of conductive devices (40; column 9, lines 45 – 50), the conductive devices formed on the bonding pads and electrically connecting the active surface of the semiconductor chip and the upper surface of the substrate (see Fig. 7D);

- a thermal enhance layer (70; column 9, lines 33 – 37) formed on the back surface of the semiconductor chip,
- wherein the substrate (10) has an opening (12; column 9, line 16) and the semiconductor chip (30) is disposed in the opening (see Fig. 7D); and
- an encapsulant (50; column 9, lines 51 – 56) encapsulating the semiconductor chip (30) and the conductive device (40) and exposing the thermal enhance layer (70).

Regarding claim 17, Shin et al. discloses in e.g., Fig. 7E and column 9, lines 33 – 37 further comprising a plurality of solder balls (60; column 7, lines 47 – 48) formed on the lower surface of the substrate (see Fig. 7E).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 3 – 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shin et al. in view of Weaver et al. (U. S. Pat. No. 6,117,352).

Regarding claims 3 – 5, Shin et al. teaches the use of the thermal enhance layer (70; Cu). Since this thermal enhance layer is made by a copper, the thermal enhance layer of Shin et al. must include an attaching material that attaches the thermal enhance layer to the semiconductor chip. However, Shin et al. does not appear to provide any example of the attaching material to be a thermally conductive polymer layer (claim 3), more specifically, a thermally conductive epoxy

film (claims 4 and 5). Weaver et al. teaches in e.g., Fig. 1, Fig. 4, column 2, lines 8 – 21 and column 6, lines 41 – 67 the attaching material (30; column 6, lines 41 – 43) of the thermal enhance layer (30; Cu and column 6, lines 41 – 44) being a thermally conductive polymer layer (34, epoxy which is a polymer; column 6, lines 48 – 51). It would have been obvious to one of ordinary skill in the art at the time when the invention was made to apply the thermally conductive epoxy layer of Weaver et al. between the chip and the thermal enhance layer of Shin et al. as taught by Weaver et al. to provide an adhesive layer between the chip and the thermal enhance layer (column 6, lines 48 – 51).

10: Claims 28, 29, 33 – 36 and 40 – 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yew et al. (U. S. Pat. No. 6,137,164) in view of Ozawa (U. S. Pat. No. 5,471,366).

Regarding claims 28, 34, 35 and 40, Yew et al. discloses in e.g., Fig. 4A a semiconductor package, comprising:

- a substrate (420; column 6, line 26) having an upper surface and a lower surface opposed to the upper surface;
- a first semiconductor chip (401; column 6, line 25) attached on the upper surface of the substrate, the first semiconductor chip having a first active surface (where the pads 411 are formed), a first back surface opposed to the first active surface and a plurality of first bonding pads (pads under the element 411; column 4, lines 55 – 57) formed on the first active surface;

- a second semiconductor chip (402; column 6, line 26) attached on the lower surface of the substrate, the second semiconductor chip having a second active surface (where the pads 412 are formed), a second back surface opposed to the second active surface and a plurality of second bonding pads (pads under the element 412; column 4, lines 58 – 60) formed on the second active surface;
- a plurality of first conductive bumps/devices (411) formed on the first bonding pads and electrically connecting the first active surface of the first semiconductor chip and the upper surface of the substrate;
- a plurality of second conductive bumps/devices (412) formed on the second bonding pads and electrically connecting the second active surface of the second semiconductor chip and the lower surface of the substrate (claim 40); and
- a plurality of solder balls (440; column 6, line 49) formed on the lower surface of the substrate (claims 34 and 35; see Fig. 4A).

However, Yew et al. does not disclose a thermal enhance layer. Ozawa teaches in e.g., Fig. 3 and column 4, line 65 – column 5, line 5 a thermal enhance layer (33-_2 and 42) formed on the back surfaces of first semiconductor chip (32-_2). It would have been obvious to one of ordinary skill in the art at the time when the invention was made to apply the thermal enhance layer of Ozawa into the structure of Yew et al. as taught by Ozawa to absorb the heat generated in the semiconductor chip (column 5, lines 30 – 33).

Regarding claims 29 and 36, Yew et al. discloses in e.g., Fig. 4A underfills (450; column 6, lines 25 – 27) disposed between the first active surface of the first semiconductor chip and the

upper surface of the substrate, and disposed between the second active surface of the second semiconductor chip and the lower surface of the substrate (see e.g., Fig. 4A).

Regarding claim 33, Yew et al. discloses in e.g., Fig. 4A the active surface of the semiconductor chip (401 or 402) facing and connecting to the upper surface of a substrate via the conductive bumps (411 or 412).

Regarding claim 41, Yew et al. discloses in e.g., Fig. 4A the first conductive devices (411) being conductive bumps, and the first active surface of the first semiconductor chip faces and connects to the upper surface of the substrate via the conductive bumps.

Regarding claims 42 and 44, while Yew et al. discloses the first and second conductive devices, and the back surface of the first and second semiconductor chips face and connect to the upper and lower surfaces of the substrate via the thermal enhance layer (450; column 6, lines 26 – 38), Yew et al. does not teach the first and second conductive devices being conductive wires. Ozawa teaches in e.g., Fig. 7 conductive wires (32x) for the conductive devices. It would have been obvious to one of ordinary skill in the art at the time when the invention was made to apply conductive wires of Ozawa on the chips of Yew et al. as taught by Ozawa to provide additional interconnections after the devices are stacked.

Regarding claim 43, Yew et al. discloses in e.g., Fig. 4A the second conductive devices (412) are conductive bumps, and the second active surface of the second semiconductor chip faces and connects to the lower surface of the substrate via the conductive bumps.

11. Claims 30 – 32 and 37 – 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yew et al. and Ozawa as applied to claim 28 above, and further in view of Weaver et al. (U. S. Pat. No. 6,117,352).

Regarding claims 30 – 32 and 37 – 39, Shin et al. and Ozawa teach the use of the thermal enhance layer (70; Cu). Since this thermal enhance layer is made by a copper, the thermal enhance layer of Shin et al. and Ozawa must include an attaching material that attaches the thermal enhance layer to the semiconductor chip. However, Shin et al. and Ozawa does not appear to provide any example of the attaching material to be a thermally conductive polymer layer (claim 3), more specifically, a thermally conductive epoxy film (claims 4 and 5). Weaver et al. teaches in e.g., Fig. 1, Fig. 4, column 2, lines 8 – 21 and column 6, lines 41 – 67 the attaching material (30; column 6, lines 41 – 43) of the thermal enhance layer (30; Cu and column 6, lines 41 – 44) being a thermally conductive polymer layer (34, epoxy which is a polymer; column 6, lines 48 – 51). It would have been obvious to one of ordinary skill in the art at the time when the invention was made to further apply the thermally conductive epoxy layer of Weaver et al. between the chip and the thermal enhance layer of Shin et al. as taught by Weaver et al. to provide an adhesive layer between the chip and the thermal enhance layer (column 6, lines 48 – 51).

Response to Arguments

12. Applicant's arguments with respect to claim 1 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is 571-272-1724. The examiner can normally be reached on 11:30 - 8:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 517-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chris C. Chu
Examiner
Art Unit 2815

c.c.
Friday, April 08, 2005

GEORGE ECKERT
PRIMARY EXAMINER